DETAILED ACTION

1. This action is responsive to the Applicant's request for a pre-appeal conference filed 12/14/07 and communication effectuated on 3/25/08.

As indicated in Applicant's above request, claims 1-23 are pending in the office action; and as a result of the above communication, there has been an agreement resulting in the following Office Action.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. Authorization for this examiner's amendment was given in a telephone interview with Att. Andrew Delizio, Reg. # 52806 on 3/25/08.

The application has been amended as follows:

In the **CLAIMS**:

4. The claims have been amended according to the Amendments herein attached as a *pdf* file entitled 'Proposed Amendments for Enabling Examiner's Amendment' as of 3/25/08, pp. 1-6 (see "Propsd_Amd_32608.pdf")

EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

5. Claims 1, 3, 6, 8-9, 11, 13, 15-16, 19-20, 23 are allowed.

The following is an examiner's statement of reasons for allowance:

The prior art taken separately or jointly does not suggest or teach the following features.

A method or computer product with program for handling register spills in a CPU having parallel registers, comprising: (i) determining that register spill instructions generated by a register allocator can be paired so to relate to corresponding register locations in each of a first register set and a second register set of said parallel registers, such that no instructions between said register spill instructions modify any of said spill instructions; (ii) modifying said register spill instructions as a parallel register spill instruction based on said determining and (iii) based on said modified parallel register spill instruction configuring storage of associated register spills in memory, wherein said configuring includes allocation space on a memory stack such that paired register spills are double word aligned; as set forth in claims 1, 9, 16, and 20.

Kolson et al, " A Method for Register Allocation to Loops in Multiple Register File Architectures", teaches coloring technique in conjunction with multiple registers organized in banks to support load (fills) and store (spills) instruction for loop iteration, and determining of what concurrent accesses can be made in said loop iteration. However, Kolson does not provide a parallel register set within a parallel register type of computer architecture in order to suggest exploiting such register set in determining as in (i) and based thereupon, modifying a paired register spill instructions to convert them into one register spill instruction using a reconfiguring of a stack based on a double word alignment, as in (ii) and (iii); e.g. the modified register spill executes the paired instructions in one parallel spill instruction.

Kahle et al, USPN: 5867684, discloses a parallel execution of a pipeline floating point loop, wherein multi-register operate in conjunction with buffers and register table to temporarily store load/store for analysis in determining based on register availability as to what such instruction can be rearranged and how to load multiple load instruction into a plurality of

registers. However, Kahle does not suggest parallel register sets and determining as in (i) for specifically pairing register spill instructions and based thereupon, modifying as in (ii) using a stack reconfiguring such as in (iii) to exploit the register disposition within parallel register architecture as set forth above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (571) 272-3735. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571)272-3759.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3735 (for non-official correspondence - please consult Examiner before using) or 571-273-8300 (for official correspondence) or redirected to customer service at 571-272-3609.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be

obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Tuan A Vu/

Primary Examiner, Art Unit 2193

March 26, 2008

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/763,512	LAPKOWSKI, CHRISTOPHER	
	Examiner	Art Unit	
	Tuan A. Vu	2193	